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XRD9827EVAL

Evaluation System User Manual

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EVALUATION KIT PART LIST

This kit contains the following:

- XRD9827EVAL Application Board
- XRD9827 20 pin SOIC
- XRD9827EVAL User Manual
- XRD9827 Data Sheet

FEATURES

- CIS or CCD Scanner Analog Front End
- Easy Evaluation of the XRD9827 20 Pin SOIC
- Accessible I/O Interface for Common Laboratory Equipment
- Optimized Layout with Four Layers

INTRODUCTION

The XRD9827EVAL is a complete printed circuit board for characterizing Exar's XRD9827. The XRD9827 is a fully integrated, high performance analog signal processor with a 12-Bit analog-to-digital converter. The XRD9827 is specifically designed for use in CIS or CCD imaging applications. CIS scanners use the S/H, PGA and digital programmable offset. CCD scanners use the CDS, PGA and digital programmable offset.

This application board combines a proven PC board layout with optimized analog and digital interface circuitry to satisfy the requirements needed in evaluating high performance devices of this type. The XRD9827EVAL contains the device being tested, latches for the output data and I/O headers for a flexible user interface. Complete AC and DC performance of the part can be evaluated by interfacing external

System Configuration-Lab Setup

The XRD9827EVAL application board is set up as a common test circuit. Figure 1. shows a block diagram of the default test configuration. See figures 2., 3. and 4. for schematic pages and circuit details.

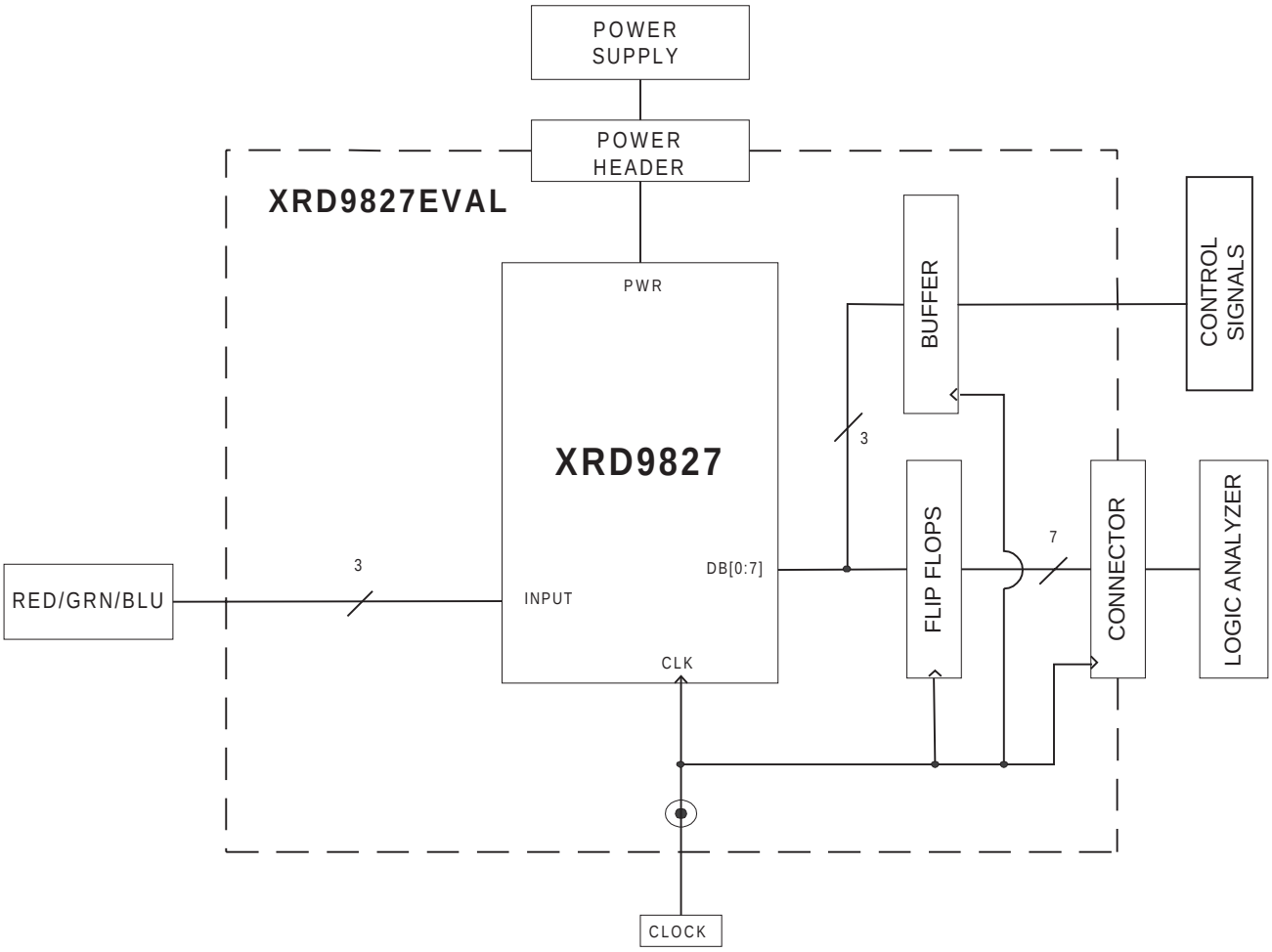

Figure 1. Block Diagram of Default Test Configuration

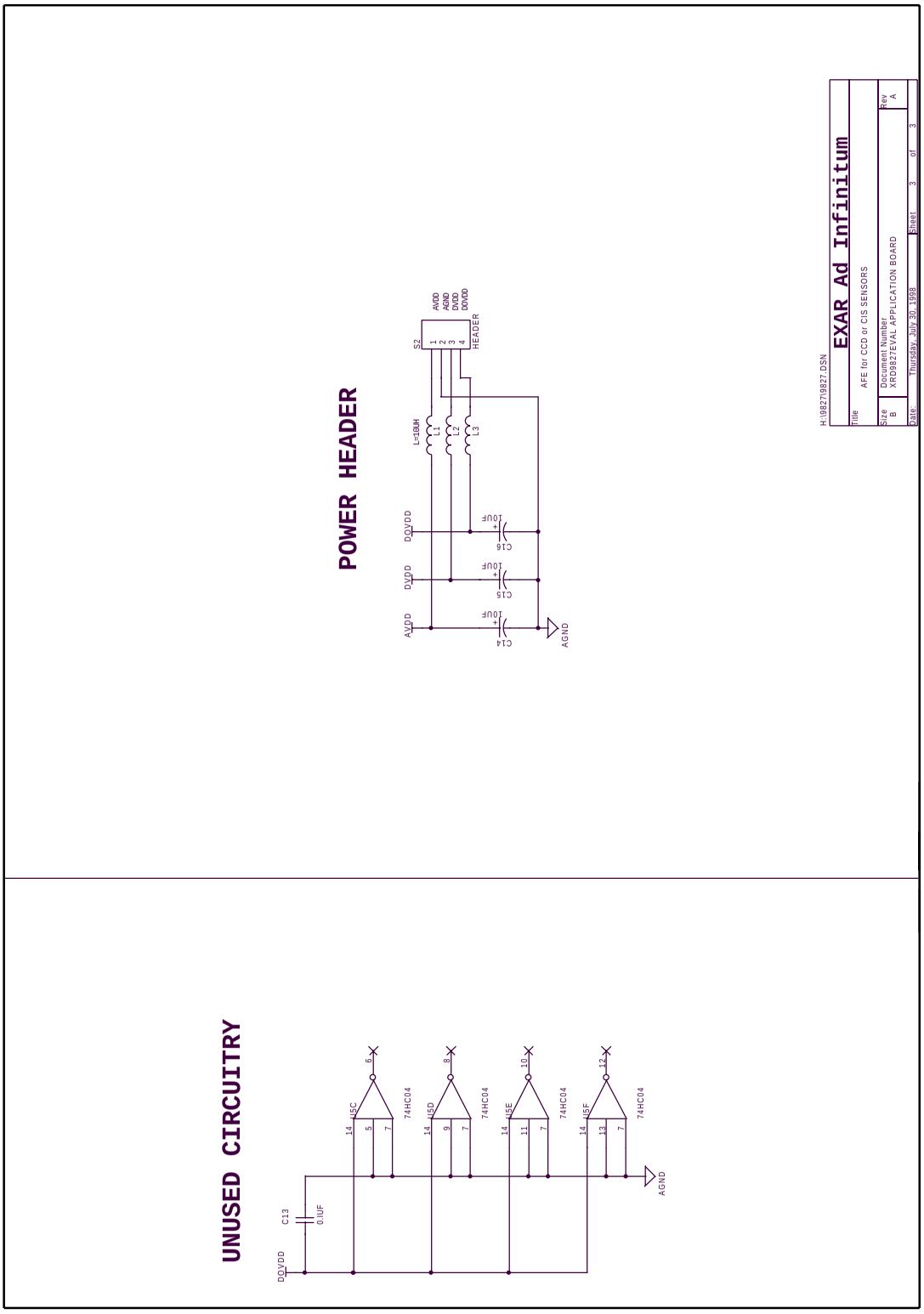

Figure 2. XRD9827EVAL Schematic Page 1.

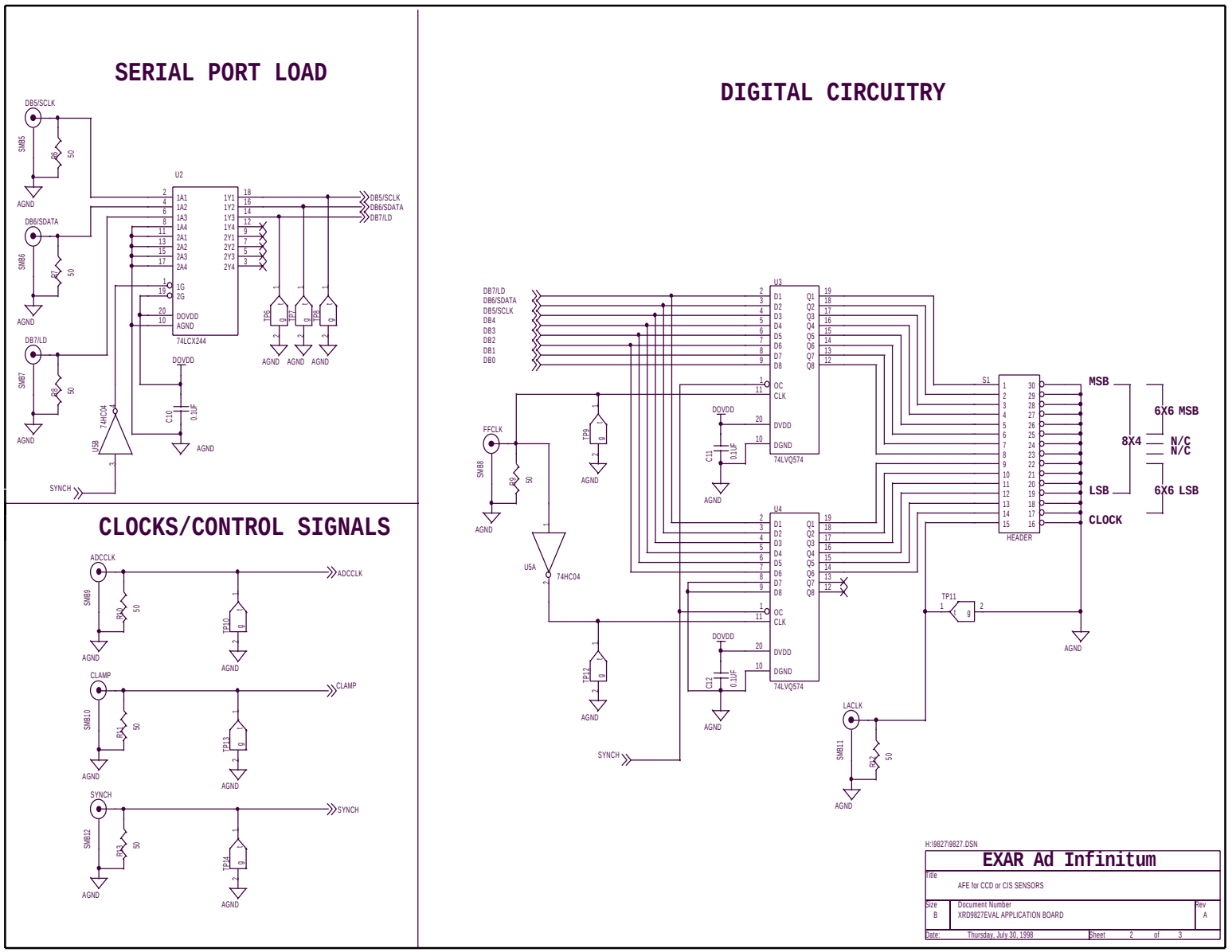

Figure 3. XRD9827EVAL Schematic Page 2.

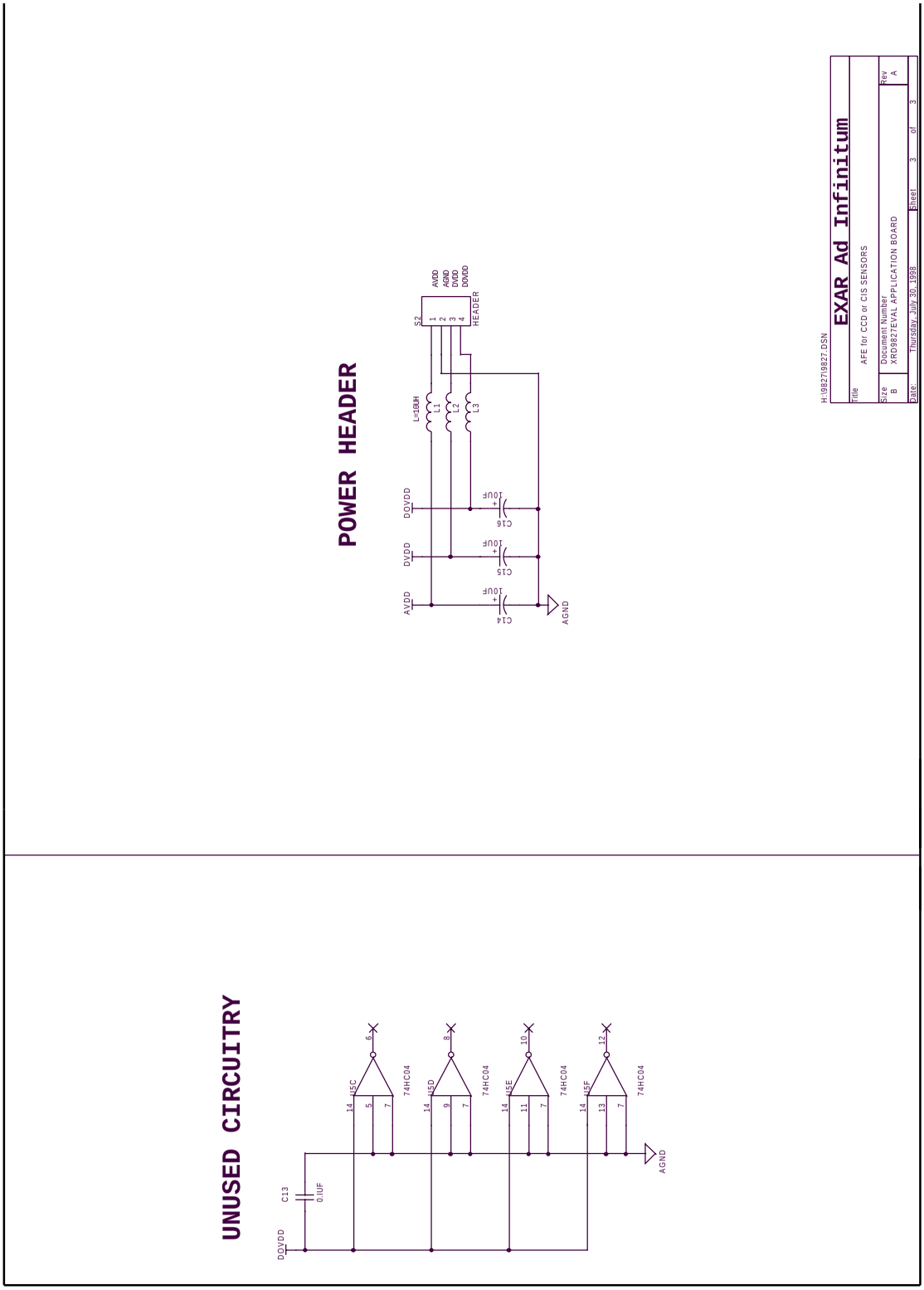

Figure 4. XRD9827EVAL Schematic Page 3.

Application Board Circuitry

Tri-State Buffer (74F244) The serial load registers are controlled by a three wire serial interface through the bi-directional parallel port to reduce the pin count of this device. When SYNCH is set to high, the output bus is tri-stated and the serial interface is activated. DB7/LD, DB6/SDATA and DB5/SCLK are tied to the 74F244 buffer which is enabled by the inverted SYNCH signal. When SYNCH is set to low, the buffer is tri-stated and the output bus of the XRD9827 returns to the output state. Below is figure 5. a simplified diagram of the buffer circuitry for loading the serial port.

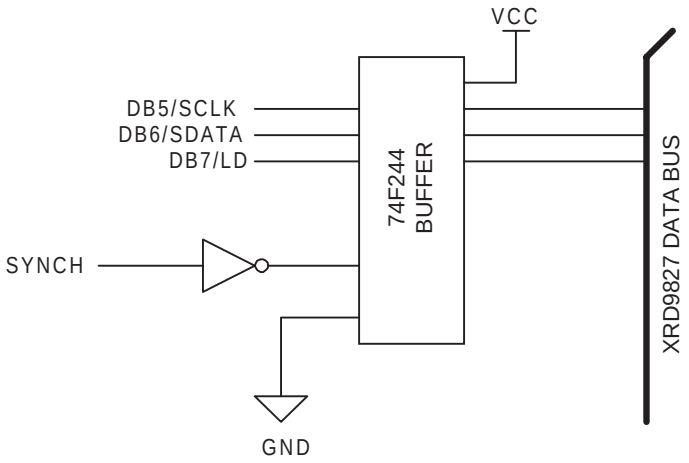

Figure 5. Simplified Diagram of the Buffer Circuitry for Loading the Serial Port

Data Output Port (74HC574)

The ADC is a 12-Bit, 10 MSPS analog-to-digital converter for high speed and high accuracy. The output of the ADC is an 8-Bit databus. The 8-Bit databus supports 6x6 or 8x4 output data. ADCCLK samples the input on its falling edge. After the input is sampled the MSB is latched to the output drivers. On the rising edge of the ADCCLK, the LSB is latched to the output drivers. The output is demultiplexed with 74HC574 Flip Flops. There is an 8 cycle latency (Config 00, 11) or 6 pixel count latency (Config 01, 10) for the analog-to-digital converter. Below is figure 6. and figure 7. a simplified diagram and timing of the digital circuitry for acquiring data from the XRD9827.

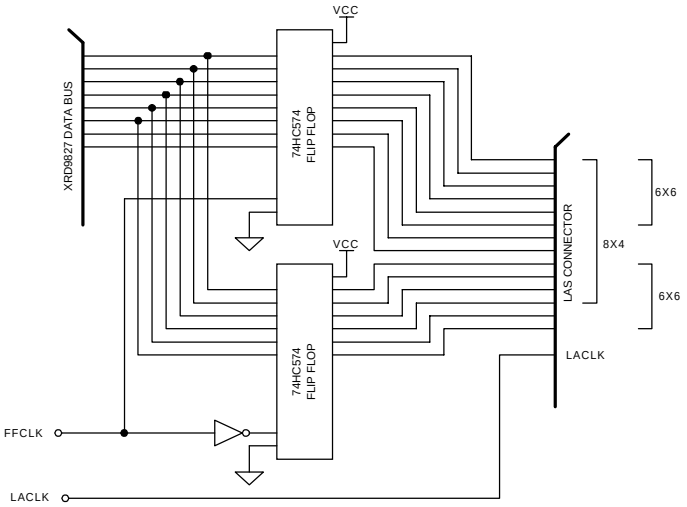

Figure 6. Simplified Diagram of the Digital Circuitry for Acquiring Data from the XRD9827

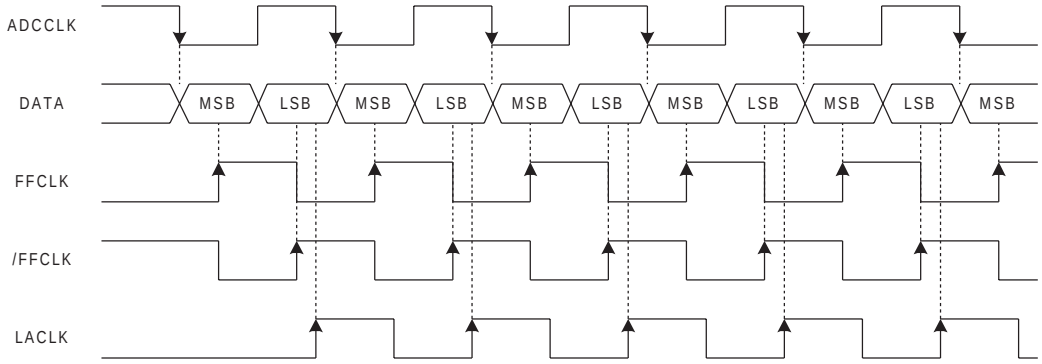

Figure 7. Timing for 74HC574s and LACLK Relative to ADCCLK

APPLICATION NOTES

Input DC Reference (VDCEXT Pin 16)

The default setting for the Input DC Reference is set to internal (Mode 110, D4=0). In this configuration, the VDCEXT node is referenced to GND. This is convenient for CIS signals with either no offset or with an offset that can be subtracted out by the internal offset DAC. If the offset of the CIS signal is larger than the 800mV offset of the internal DAC, configure the Input DC Reference to external (Mode 110, D4=1). In the external Input DC Reference configuration two applications are possible.

Application #1. VDCEXT as an Input:

An external DC reference can be applied to VDCEXT Pin 16 that can be used as an offset to subtract out any DC offset inherent to the CIS signal (Mode 110, D4=1) and (Mode 111, D4=0). For example: If the CIS signal has a dark offset of 1.5 volts, a voltage divider can be used to supply 1.5 volts to VDCEXT to cancel out the DC offset. Below is Figure 8. the typical application circuitry for applying a DC offset externally to the XRD9827 (Pin 16).

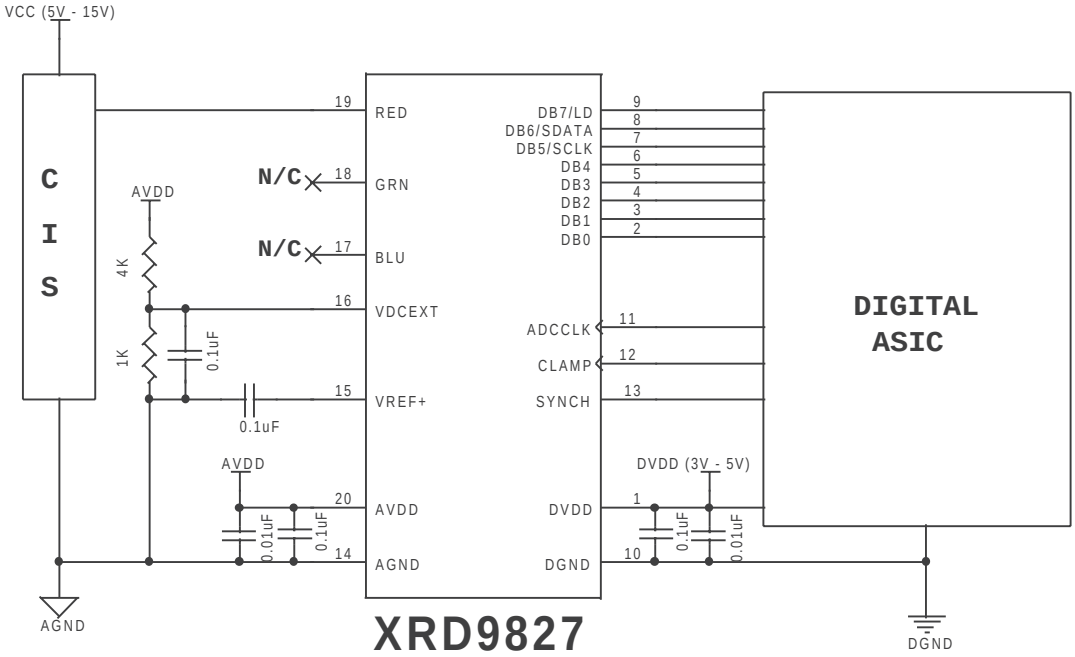

Figure 8. Typical Application Circuitry for Applying DC Offset Externally to VDCEXT (Pin 16)

Application #2. VDCEXT as an Output

By setting the Input DC Reference to external, the internal band gap voltage can be used by setting the Internal CIS Reference Circuit to Reference Circuit Enabled (Mode 110, D4=1) and (Mode 111, D4=1). Note: The Internal CIS Reference Circuit is intended to be used with the Canon CIS Model #CVA-60216K. In this configuration, VDCEXT becomes an output of 1.24 volts. This voltage can be directly connected to the VREF (Pin 5) of the Canon CIS sensor. This reduces the amount of components needed for this application. The diodes and resistors typically used in this application to provide this reference have been included inside the XRD9827 for this mode of operation. Below is Figure 9. the typical application circuitry for interfacing to the Canon CIS Sensor Model #CVA-60216K.

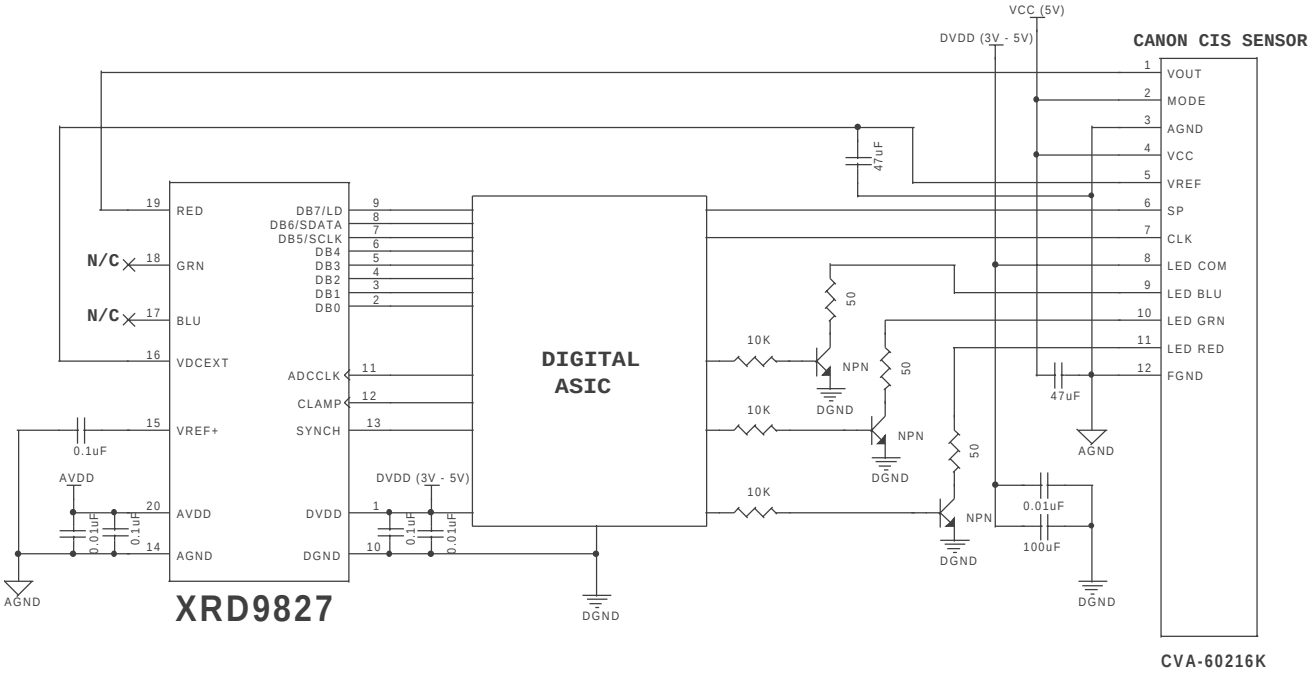

Figure 9. Typical Application Circuitry for Interfacing to the Canon CIS Sensor Model #CVA-60216K

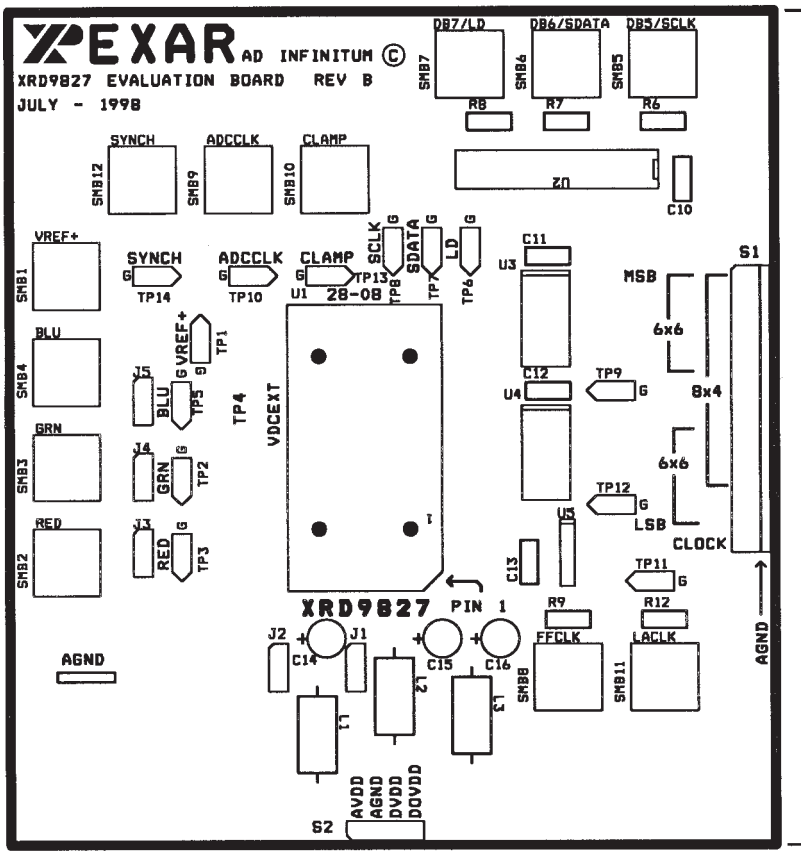

Figure 10. XRD9827EVAL Top Silk Screen

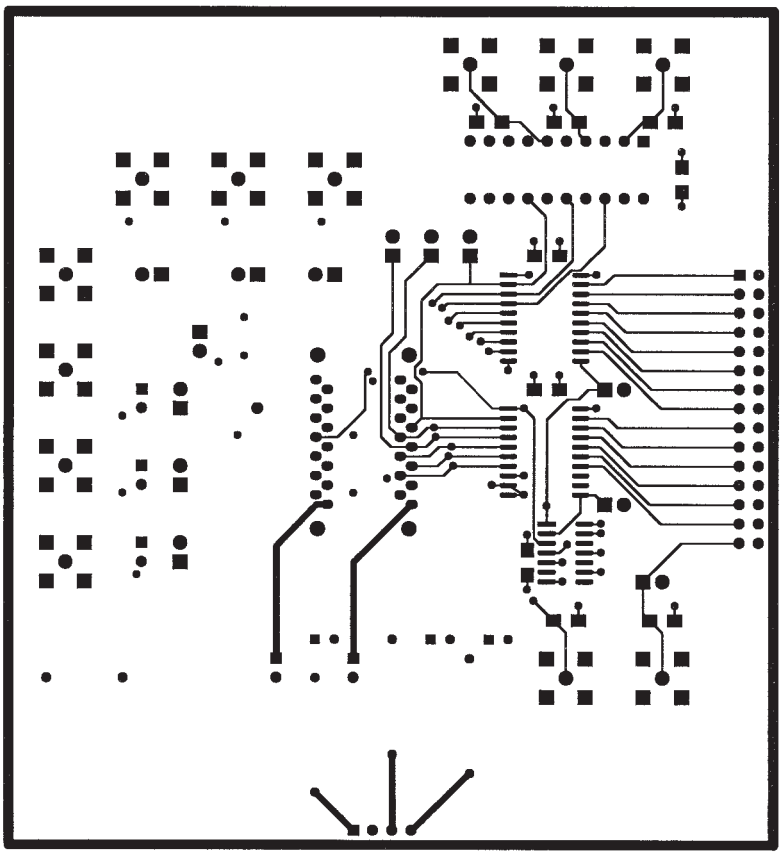

Figure 11. XRD9827EVAL Top Layer

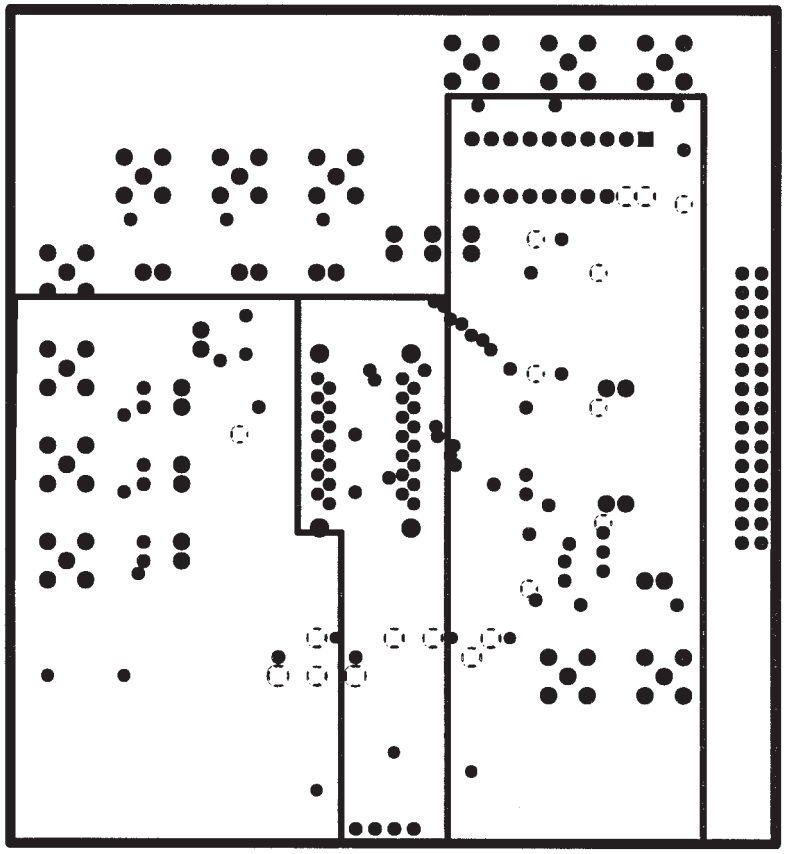

Figure 12. XRD9827EVAL Ground Plane

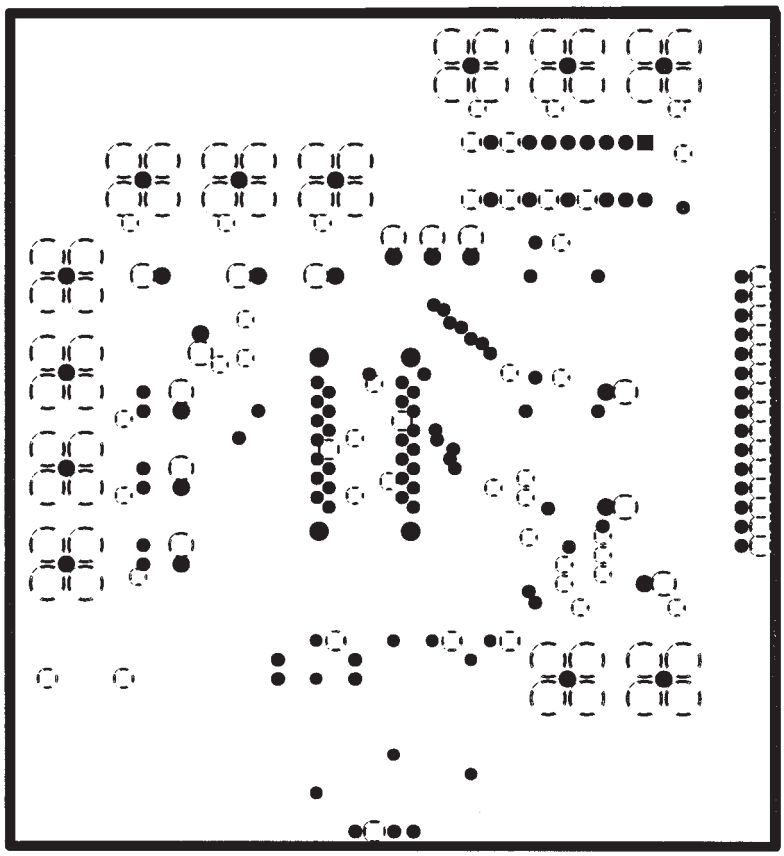

Figure 13. XRD9827EVAL Power Plane

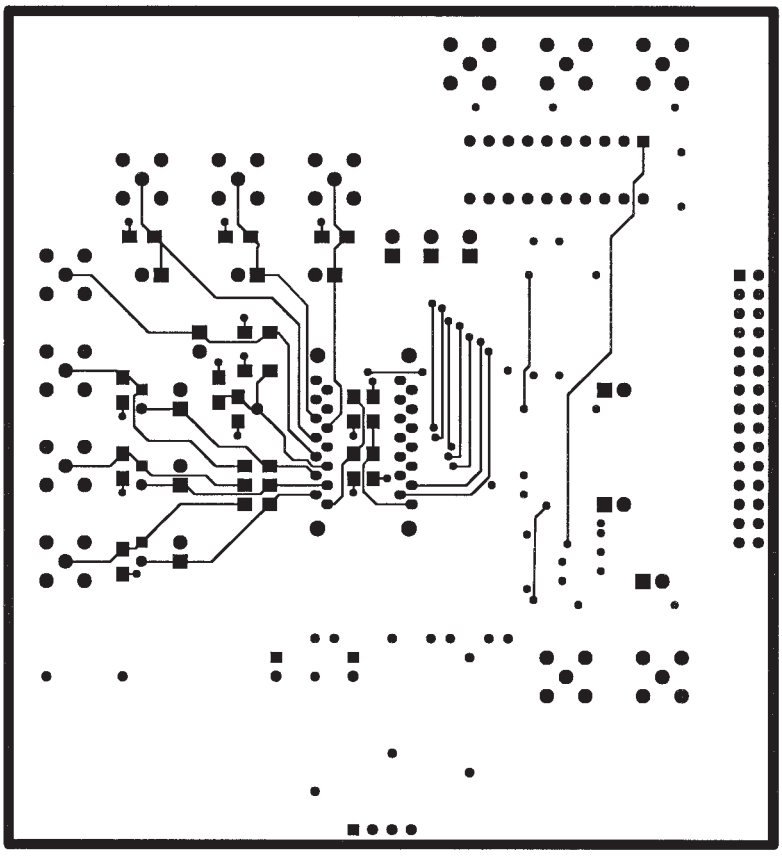

Figure 14. XRD9827EVAL Bottom Layer

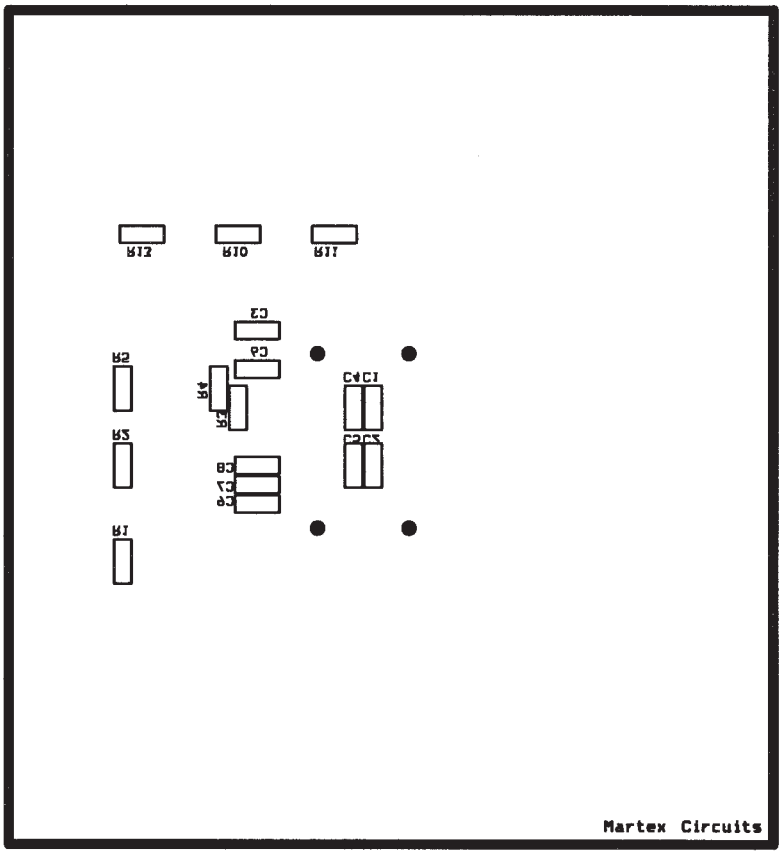

Figure 15. XRD9827EVAL Bottom Silk Screen

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